SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

RESISTANCE TO SOLDERING HEAT AND THERMAL CHARACTERISTICS OF PLASTIC SMDs

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INTRODUCTION

Surface Mount Technology (SMT) has introduced a number of new technical problems, which have delayed the conversion from insertion assembly.

This is not strange : what readily available source of expertise existed a few years ago ?

Plastic SO packages were introduced in Europe in the early '70s and widely used in hybrids, but hybrid assembly has little relationship with the placement, soldering, handling tools now considered for SM PCB production. Was it surprising that even the semiconductor suppliers with sound experience in SO production could not give all of the answers needed by the PCB manufacturer ?

Japanese experience in SMT based consumer products is impressive : 87% of components used for cameras are in SM versions. However, the degree of complexity and performance of consumer products are somewhat different from the industrial, automotive and telecoms applications the Western world is interested in. On the other hand, in 1985 the percentage of SMDs (active and passive) used in industrial systems produced in Japan was 16.6% in telephones, 5.5% in automotive applications, 5.1% in cable communication, 0.7% in minicomputers[1] ; that is, a level similar to US and European production, presumably with a similar level of expertise.

In the past few years confidence in SMT has increased. More experience exists, which is the result of an expensive learning phase covered by both SMD manufacturers and users.

The reliability of plastic SMDs has an important place in this work. It needs a new approach in comparison with equivalent insertion devices, due to the completely different use.

In 14 years of production, no distinction was made in the authors' company between SO and DIP, from the point of view of reliability. They had the same reliability targets and similar evaluation methodology ; the former was often hot plate soldered on leaded ceramics for more convenient handling but no difference in long-term reliability existed.

With SMT, this is inadequate. Negative effects due to the various assembly processes, and to some thermomechanical influence of the board, can limit the device life.

The present work is focused on SMDs soldered onto a plastic substrate, by means of the most common industrial processes, and takes into account two aspects of reliability :

1. Resistance to soldering heat, i.e., the suitability to withstand the thermal shock associated with the soldering cycle, without reducing reliability. This information is obtained by performing moisture resistance tests. Data about SO packages will be presented. For PLCCs, evaluation is in progress and will be concluded in the first half of 1988.
2. Heat dissipation, which influences the failure rate. This information is obtained with test patterns and test boards designed by SGS-THOMSON Microelectronics and includes thermal impedance in pulsed conditions. A few case studies will be included in this paper but complete characterisations are available elsewhere.[2]

RESISTANCE TO SOLDERING HEAT

In through-hole technology, devices are inserted from the upper side of the board and wave soldered from its lower side.

Only the lead extremities reach the temperature (250-260°C) of the molten solder ; the maximum specified soldering time of 10s is short enough to avoid over-heating of the package body, which generally does not exceed 120-130°C during the whole process.

This temperature is lower than the moulding compound glass transition temperature (160-170°C) and the risk of permanent damage to the package structure or to the silicon die is excluded.

Device reliability is defined almost independently of the soldering time and temperature ; devices under reliability test are mounted on sockets, thus neglecting the effect of the assembly process.

On the contrary, in all industrial SMT processes, devices are soldered in a high temperature ambient (215-260°C), with high heating rate, and the plastic package is kept in glass transition conditions

(figure 1) for a relatively long time (up to 60s). This situation was never encountered before.

Concern over reduced reliability is justified and explains the trend towards defining SMD reliability *after* the soldering cycle, in order to include the effects summarised in table 1.

Figure 1 : Thermal Expansion of Moulding Compounds, Compared with the Temperature of Different Soldering Techniques.

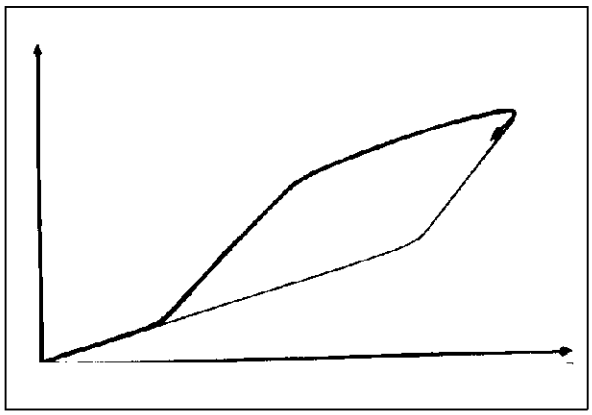


Table 1 : Factors Affecting SMD Reliability on Printed Board.

SMD Package	
Design and Structure	Volume and Thermal Inertia
Internal Contamination	Water Content
Thermomechanical Properties	Lead Solderability
Assembly Process	
Soldering Method	Contamination Level (flux)
Soldering Time/temperature	Rinsing
Substrate	
Thermomechanical Properties	Thermal Dissipation

EXPERIMENTAL

Reliability tests are performed on parts soldered onto test boards (4.5 in. x 6.5 in. FR-4 substrates).

SM PCB1 test board can accept SO-8, 14, 16. It is pre-grooved, in order to be cut in 35 positions, having the lay-out shown in figure 2 ; the SMD footprints are electrically connected to through-holes, with a pitch of 100 mils and placed in two parallel rows, 600 mils apart. Commercial pins inserted in the through-holes give the possibility of using the same equipment needed by DIPs.

The soldering processes from table 2 were used for SO packaged bipolar Operational Amplifiers and C-Mos Standard Logic. In order to simulate a rework, the soldering cycle was repeated on a number of devices. Soldering is followed by the usual rinsing in water or Freon, with or without ultrasonics.

Figure 2 : SM PCB1 Test Board.

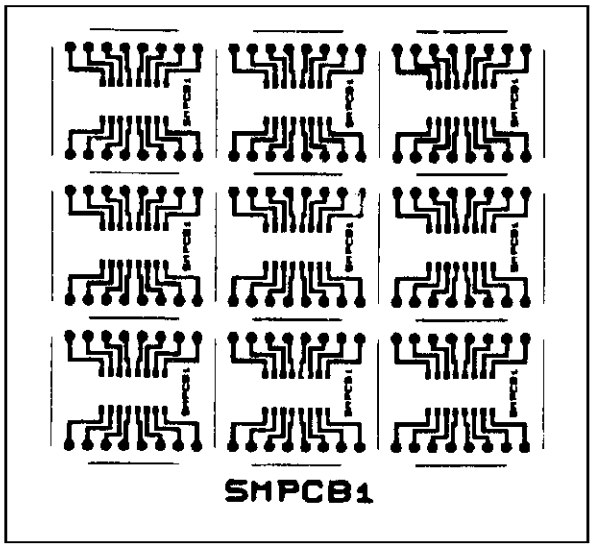


Table 2 : Soldering Processes Evaluated with SO Packaged Devices.

	Pre–heating	Soldering	Number of Cycles
Double Wave	120°C/30s	225°C/4s	1
Double Wave	120°C/30s	250°C/4s	1
Double Wave	110°C/30s	250°C/3.4s	1, 2, 3, 4
Triple Wave	110°C/30s	260°C/3s	1, 2, 3
Vapour Phase		215°C/20s	1, 2
Infra-red	160°C/30s	> 210°C/60s	1

The reliability evaluation was performed by means of the following tests :

Operating Life	150°C
Pressure Pot	121°C/2atm
THB	85°C/85% RH 15V (bips) 6V (CMos)
HAST	130°C/85% RH 15V (bips) 6V (CMos)
Thermal Cycles	– 55/+ 150°C (30/5/30 min)
Thermal Shocks	– 55/+ 150°C (5/1/5 min liquid)

130°C/85%RH Highly Accelerated Steam Test (HAST) has an acceleration factor of about 18-20 (ref. 3) in comparison with 85C/85%RH, and the concrete possibility of reaching wear-out exists with this test, after an acceptable time.

For PLCC packages a similar methodology is followed. At the time of writing, only partial data are available, which will not be included here.

EXPERIMENTAL RESULTS

Experimental results are summarised in tables 3-6.

Table 3 : Cumulative Reliability Data after Multiple Wave Soldering.

Test Vehicles : LM2904 (SO-8), LM2901 (SO-14) and M74HC74 (SO-14)		
Double Wave	225°C/4s	250°C/4s
Triple Wave		260°C/3s
Operating Life 1000h	0/154	0/32
Pressure Pot 96h	0/104	0/62
THB 85°C/85%RH 1000h 2000h	1/105*	0/32 0/32
HAST 130°C/85%RH 100h 200h		0/64 0/64
Thermal Shocks 500	0/231	0/77
* Parametric Failure		

Table 4 : Reliability Data after Vapour Phase Reflow.

Test Vehicle : LM2901 (SO-14)		
	215°C/20s	215°C/40s
Operating Life 1000h		0/32
Pressure Pot 96h		0/32
THB 85°C/85%RH 1000h 2000h		 0/32 0/32
HAST 130°C/85%RH V = 15V 100h 200h 372h 458h 635h	 0/56 0/56 0/24 2/24 5/22	 0/12 0/12 1/12 1/11 3/10
Thermal Cycles 500		0/32
All failures due to pad corrosion		

Table 5 : Cumulative Reliability Data after Infra-red Reflow.

Test Vehicles : M74HC00 and M74HC74 (SO-14)	
	> 210°C/60s
Operating Life 1300h	0/34
THB 85°C/85%RH 1300h	0/34
HAST 130°C/85%RH 100h 200h 500h 672h	 0/32 0/32 0/32 0/32
Thermal Cycles 750	0/70

Table 6 : Cumulative Reliability Data in Multiple Wave Soldering with Repetition of the Soldering Cycle.

Test Vehicles : LM2903 (SO-8), LM2901 and M74HC00 (SO-14)							
		Double Wave 250°C/3.4s			**Triple Wave 260°C/3s**		
Number of Cycles	1	2	3	4	1	2	3
Pressure Pot 96h 504h		 0/56 0/56					
100 Thermal Cycles (– 40/150°C) Followed by Pressure Pot 96h 168h 240h					 0/30 0/30 0/30	 0/30 0/30 0/30	 0/60 0/60 0/60
HAST 130°C/85%RH V = 6V 100h 500h 1000h 1150h 1300h	 0/32	 0/32	 0/32 0/18 0/18 1/18 17/1	 1/32* 0/18 0/18 1/18** 17/1			
* Parametric Failure ** Pad Corrosion							

COMMENTS ON THE RELIABILITY RESULTS

Previous results do not reveal negative effects due to the exposure of SM devices to the soldering heat, for all of the industrial SMT soldering methods, in combination with the most common solders and cleaning solvents (Freon, water with and without ultrasonics).

Wear-out in the HAST test (130°C/85%RH) is between 1100 and 1300 hours when the soldering cycle is repeated up to 4 times with high temperature (250-260°C) multiple wave soldering, which is considered to transfer the highest thermal stress to the package body.

Pad corrosion is the final failure mechanism for all samples.

This performance is about 7-10 times better than the 2000-3000 h THB 85°C/85%RH, which is currently requested as qualification target in moisture resistance biased tests. Therefore, the reliability of surface mounted devices considered in this work is high enough to meet the most stringent requirements of the professional market.

No evidence of cracks in the plastic case was found in the previous evaluations. This effect (referred to also as 'pop corn' effect) is attributed to some ano-

malous thermal expansion of the package in the soldering phase, caused by water absorbed by the plastic encapsulation : a thermal treatment at a temperature higher than 100°C for a few hours is suggested in order to remove the absorbed water.[4]

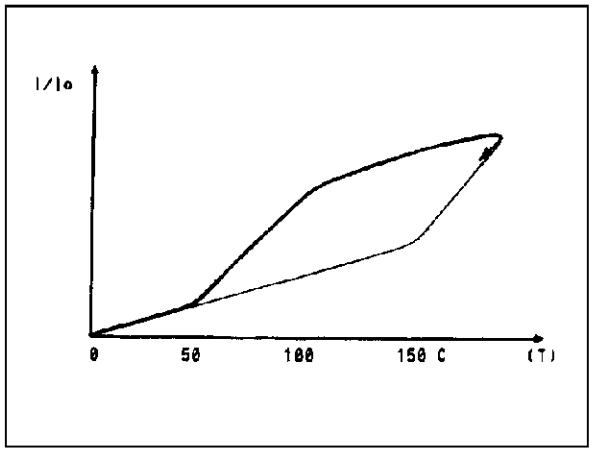
As this thermal pre-conditioning should be performed shortly before soldering, a serious problem arises in the assembly line. Such thermal annealing is not practical when the parts are supplied in plas-tic tapes or sticks : they should be removed from the packs by the user, heat treated, and packed again with additional costs and risks (co-planarity).

In this company's experience, the 'pop corn' effect can be completely avoided by controlling the frame-encapsulant interface, which is the easiest path for the water. Furthermore, experience has indicated that water at that interface does change the expansion characteristics of the package. About five years ago, the curve of figure 3 was found in some parts (coming from lots affected by the 'pop corn' problem) using Thermo-Mechanical Analysis (TMA). Devices under test were placed between the probes of the TMA transducer and their expansion characteristics recorded.

In the first ramp (5°C/min), package expansion was much higher than the moulding compound expansion between 50 and 100°C ; over 100°C, it returned on the curve typical of the encapsulant. Cooling down and repeating the measurement, only the lower curve of figure 3 was covered.

This behaviour was attributed to water having penetrated between the frame and the plastic body, whose expansion was responsible for the package deformation during the slow heating in TMA. When the parts were soldered on the substrate, cracks could occur due to the much faster heating rate.

Figure 3 : Thermal Expansion of SO Packages.



The problem was solved when the possibility of controlling the water content was found, by means of an improved frame design and some dedicated production steps.

Millions of parts assembled in recent years showed no evidence of the 'pop corn' effect, without any pre-conditioning before use.

The same solutions are successfully adopted for PLCC packages.

THERMAL CHARACTERISTICS

Correlation between reliability and junction temperature Tj is known :

the device lifetime is roughly halved when Tj is increased by 10°C.

Mainly due to this fact, thermal dissipation is a second factor which can influence SMD reliability : a reduced body means worse dissipation and higher power density on the board.

As careful thermal design is the key to improved reliability, a systematic characterisation of SM packages was performed, in order to study the main factors affecting thermal dissipation at both levels of package design and board design.

In the course of this work, the need for some critical revision of the way of producing and using thermal data was evident.

A point which cannot be under-evaluated is the choice of measurement method, as will be discussed later.

Another important point is the following : the common way of specifying the junction to ambient thermal resistance Rth(j-a) is to associate one value of Rth(j-a) to each device.

In the majority of data books, including this company's previous literature, little information is given on the experimental conditions used to obtain that value : the dissipated power and , above all, the kind of interconnection between the package and the measurement set-up (wires, socket or board), which in some cases can become a far from negligible heat transfer element.

Ignoring this contribution was probably justifie with packages having a low thermal conductivity frame, such as Alloy 42 or Kovar.

For those packages, heat spreading was limited to the silicon die and to the die pad ; thermal dissipation was little affected by the surroundings and the measurement assembly had little influence on the final value of Rth(j-a).

This is not the case concerning the same packages with a copper frame, introduced a few years ago to achieve a higher power capability ; due to better thermal conductivity of the leads they are much more sensitive to external dissipating media, eventually used for the measurement.

Similar statements are valid for SMDs and become more important on account of their reduced dimensions.

The concept is summarised in table 7, where the thermal resistance of some dual-in-line (DIP), Small Outline (SO) and Plastic Leaded Chip Carrier (PLCC) packages is given. The influence of the frame thermal conductibity is remarkable ; but likewise remarkable are the differences obtained for the same package, when it is connected by thin wires (and 'floating' in still air) or soldered on a PC board during the measurement.

Table 7 : Junction to Ambient Thermal Resistance (C/W) for DIP and SM Packages in Different Experimental Conditions.

	Power Pd[W]	'Floating' in Air	On SGS Test Board	Ratio
DIP 14 Leads (*)				
Alloy 42 0.25mm	0.5	156	138	1.13
Cu 0.25mm	0.6	125	90	1.39
SO-14 Leads (**)				
Alloy 42 0.25mm	0.4	280	195	1.43
Cu 0.25mm	0.6	190	105	1.80
PLCC-44 Leads (***)				
Cu 0.25mm	1.0	70	52	1.35
die size :	(*) = 0.095 in. x 0.110 in. (**) = 0.060 in. x 0.090 in. (***) = 0.180 in. x 0.180 in.			

Especially for SO packages the influence of the substrate on thermal dissipation is noticeable. This fact can help to explain the following points :

1. The Rth(j-a) values published by different SMD suppliers are distributed in too wide a range (more than 70°C/W for SO packages) which handicaps a correct thermal design. Most of the difference is probably due to different test boards, and the availability of standardised measurement methodology should help to give more accurate information.
2. The board lay-out contribution should be studied, in order to quantify the effect of device density : a suitable distance between two or more dissipating elements can be an effective solution for improved reliability.
3. Specification of thermal characteristics should include more elements (power level, board density, package design) which cannot be summarised in one single thermal resistance value, as was commonly the case with Alloy 42 DIPs.

A set of experimental curves was obtained for each SM package,[2] which gives the relationship between these factors ; if used to feed back the board de-sign, they should help to achieve a better thermal performance.

The most significant results will be discussed here.

Moreover, two other factors will be considered.

1. The thermal capacitance of the package, which is significant especially in higher pin count PLCCs ; it delays Tj increase during power transients and is important in switching applications.
2. The frame design in association with a suitable board design ; a low resistance thermal path can be obtained with modified frames ; heat is then conveyed to copper areas obtained on the board and dissipated power can be increased to 2W with SOs and PLCCs.

EXPERIMENTAL METHOD

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method : at present, only draft specifications[5] exist, proposed in 1986 and not yet standardised.

The experimental method used in this company since 1984 has anticipated these preliminary recommendations to some extent, as it is based on the P432 thermal test pattern (figure 4) having two npn transistors, with 10W each power capability. A sensing diode is placed on the thermal plateau arising when the transistors are operating in parallel and gives the actual value of Tj, through the calibration curve of its forward voltage Vf (at constant current) vs temperature.

Transistor size, which is not fixed by the documents proposed for standardisation, was intentionally limited to 1000 mils^2, in order to simulate a high power density and characterise the worst case. Die size, which is found to have some influence on thermal resistance when copper frame is used, is slightly smaller than the die pad size and never exceeds 30000 mils^2 in larger packages, such as high pin count PLCCs.

The measurement set-up is shown in figure 5. It is compatible with DC and AC power supply and has an accuracy better than 5%.

The advantages offered by the test pattern are :

(i) high power capability (wider evaluation range) ;

(ii) repeatable electrical characteristics (Vf) and temperature coefficient (1.9mV/C) of the sensing element (accuracy) ;

(iii) high resolution in pulsed conditions (evaluation down to 100s pulses) ;

(iv) better correlation from one package to another.

Alloy 42 frames and copper frames were used for narrow SO packages (150 mils body) ; only copper frames were considered for the others : wide SO (300 mils body) and PLCC packages.

Suitable FR-4 test boards were developed, which will be described case by case.

Figure 4 : Test Pattern P432 Layout.

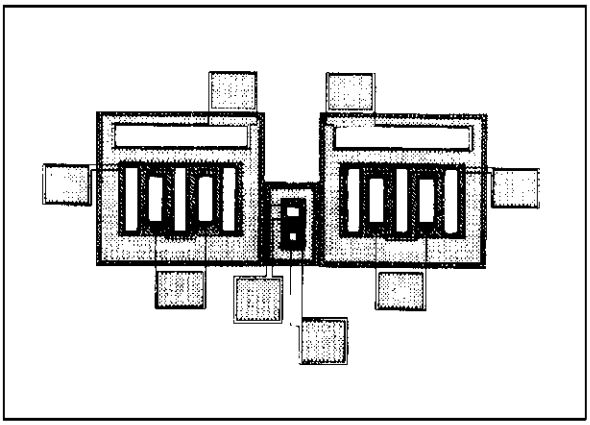
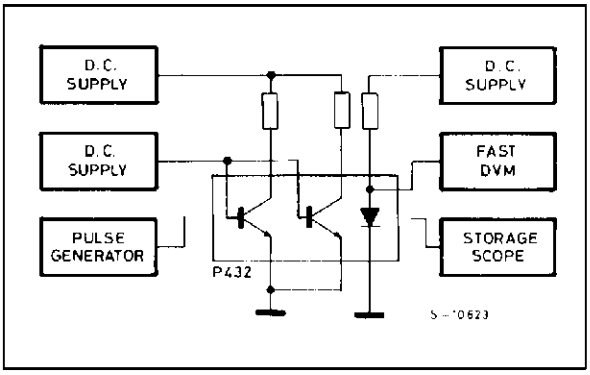


Figure 5 : Measurement System.



THERMAL CHARACTERISTICS IN DC CONDITIONS

Thermal characteristics of the SO-14 package in DC conditions are shown in figure 6.

The upper curve is related to samples floating in still air and connected to 8 thin wires needed for biasing the dissipating transistors and the sensing diode of the P432 test pattern.

Samples soldered on the FR-4 test board shown in figure 2 have an approximately halved thermal resistance ; by reducing the copper pattern length of the test board, different component densities are simulated : thermal resistance is increased by about 30% when the track length has the minimum value.

Dependence of the thermal resistance on the total area of the traces connected to the package is represented by the curve of figure 7. It quantifies the effectiveness of the board lay-out to spread the heat and dissipate it towards the ambient and can be conveniently used for determining the thermal resistance value associated with a given board design.

Figure 6 : Rth(j-a) of SO-14 Package vs. Power Level.

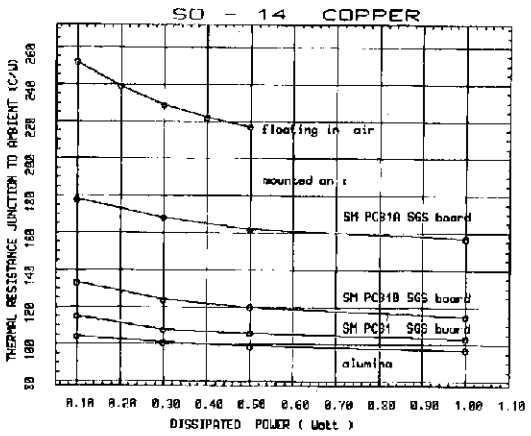


Figure 7 : Rth(j-a) of SO-14 vs. on Board Trace Area.

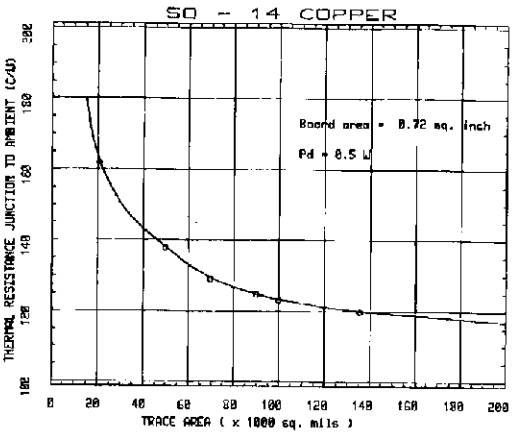
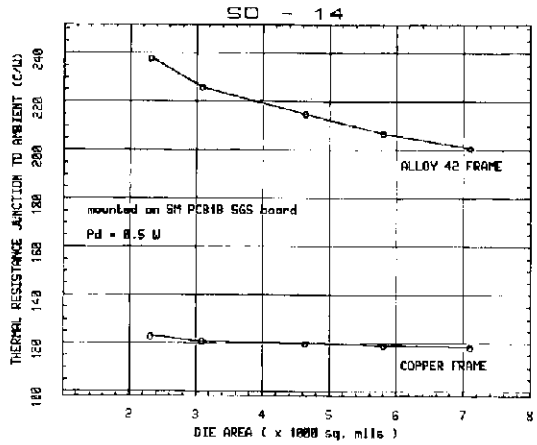


Figure 8 : Rth(j-a) of SO-14 with Copper (SGS-THOMSON) and Alloy 42 Frame.



Comparison of low conductivity (Alloy 42) and high conductivity (copper) frames is shown in figure 8.

The data obtained for the different SM packages are summarised in table 8 ; the two thermal resistance values refer to the two extreme cases of a low density and a high density board.

Table 8 : Summary of Junction to Ambient Thermal Resistance in Steady State Power Dissipation (SGS-THOMSON test boards)

	Die Pad Size (milinches)	Power Pd [W]	Rth(j-a) [°C/W] on Board
SO-8 Alloy 42	90 x 100	0.2	250-310
Copper	95 x 100	0.2	160-210
SO-14 Alloy 42	98 x 118	0.3	200-240
Copper	78 x 118	0.5	120-160
Copper	98 x 125	0.7	105-145
SO-16 Alloy 42	98 x 118	0.3	180-215
Copper	94 x 185	0.5	95-135
SO-16W Copper	120 x 160	0.7	90-112
SO-20 Copper	140 x 220	0.7	77-97
PLCC-20 Cu	180 x 180	0.7	90-110
PLCC-44 Cu	260 x 260	1.5	50-60
PLCC-68 Cu	425 x 425	1.5	40-46
PLCC-84 Cu	450 x 450	2.0	36-41
Rth(j-a) values correspond to low and high board density			

THERMAL IMPEDANCE IN PULSED CONDITIONS

The electrical equivalent of heat dissipation for a module formed by the active device, its package, the board and the external ambient is a chain of RC cells each having a characteristic risetime $\tau = RC$.

Thermal capacitance is the capability of heat accumulation and depends on the heat capacitance of the materials, their volume and their density.

When the power is switched on, the junction temperature after a time t is the result of the subsequent charge of the RC cells, according to the well known exponential relationship :

$$\Delta T_j = Rth \times Pd \times (1 - et/\tau)$$

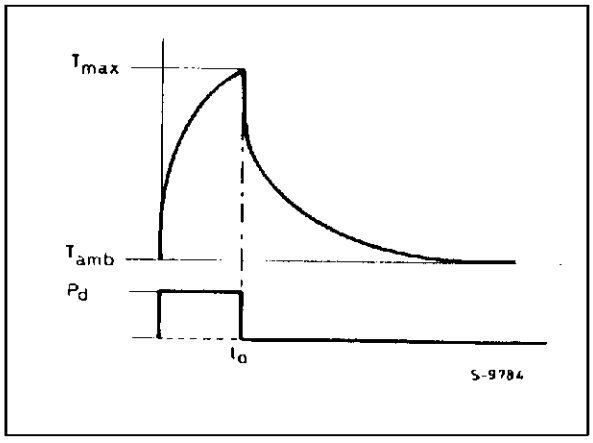
When the pulse length t_o is an assigned value, effective T_j can be significantly lower than the steady state T_j (figure 9) and a transient thermal resistance $Rth(t_o)$ can be defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Obviously, for shorter pulses, transient thermal resistance is lower and a higher power can be dissipated without exceeding the maximum junction temperature defined in reliability considerations.

In a similar way, when pulses of the same height Pd are repeated with a defined duty cycle DC and the pulse is short in comparison with the total risetime of the system, the train of pulses is seen as continuous source at a mean power level :

$$Pd_{avg} = Pd \times DC$$

Figure 9 : Qualitative Tj Increase for Single Power Pulse.



On the other hand, the silicon die has a risetime of 1-2ms and is able to follow frequencies of some kHz : junction temperature oscillates about the average value :

$$\Delta T_{javg} = Rth \times Pd_{avg}$$

as qualitatively shown in figure 10.

The thermal resistance corresponding to the peak of the oscillation at the equilibrium (peak thermal resistance) gives information on the maximum temperature reached by the device and, depending on DC and pulse width, can be much lower than DC thermal resistance.

Figure 10 : Qualitative Tj Increase for Repeated Power Pulse.

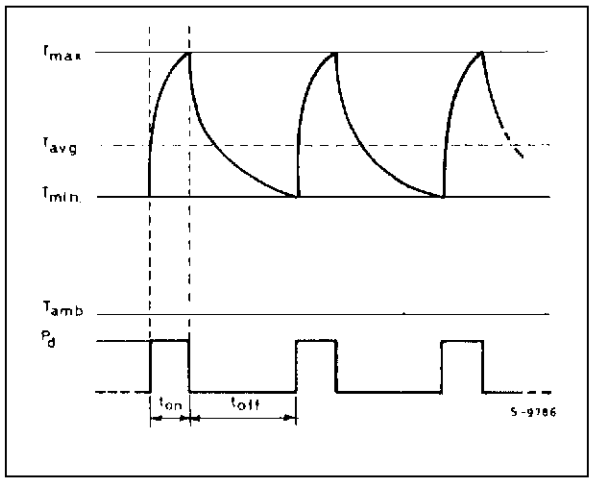
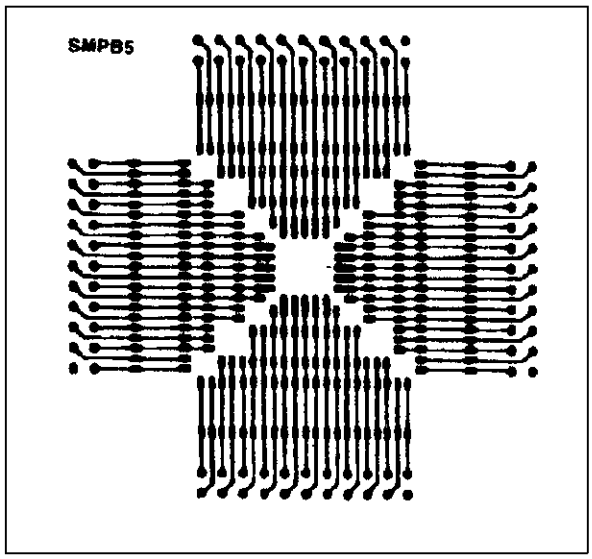
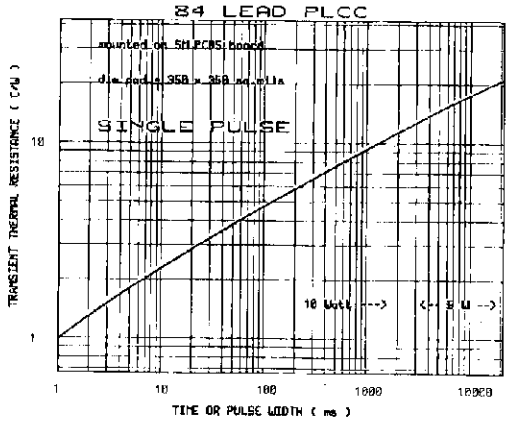


Figure 11 : Test Board for PLCC.



The knowledge of thermal characteristics in the AC condition is a valid tool to reduce redundancy (and cost) in the thermal design of pulsed applications.

Figure 12 : Transient Thermal Resistance for PLCC-84 on Board.



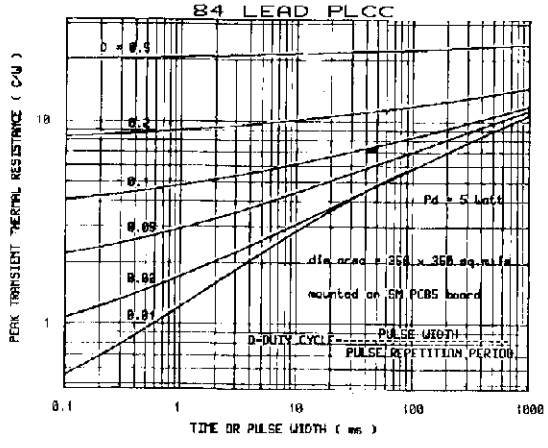
The example is now given of a high pin count PLCC, which has a large thermal capacitance, due to its volume and weight.

Temperature increase for 84 lead PLCCs soldered on the SM PCB5 test board (figure 11) for single pulses of different length is given in figure 12. A risetime of 50-60s is typical for this package, having a thermal resistance of 38°C W in steady state (see table 8).

For single pulses, the effective thermal resistance is much reduced and acceptable junction temperature is observed even for high power pulses. 10W can be delivered for about 1s (9°C/W) and 5W for 10s (18°C/W).

Peak thermal resistance for repeated pulses, with different duty cycles, is represented in figure 13 and the above considerations are valid in this case also.

Figure 13 : Peak Transient Rth for PLCC-84 on The Board.



MEDIUM POWER APPLICATION

The lack of power packages suitable for SMT requirements (standard outline, automatic handling) is known.

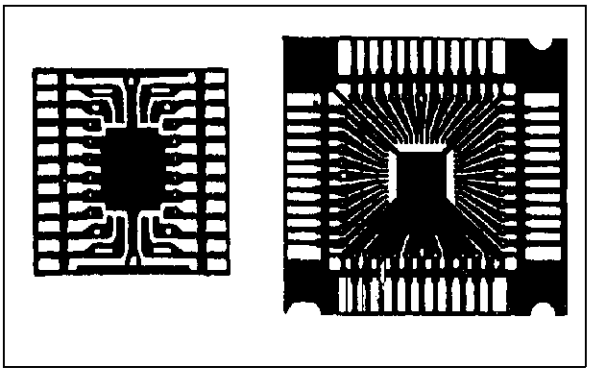
A simple way to achieve power dissipation in the medium range (1-2W) is to transform the available signal packages and modify their frame to obtain a high conduction path.

In figure 14 the frame of medium power SO and PLCC packages is shown : some leads are connected to the die pad, in order to have a low junction-to-pin thermal resistance Rth(j-p). Typical values of this parameter are in the range of 12-15°C/W, with a high conductivity lead frame.

Modification involves the internal part of the frame only, while the external dimensions of the package are not changed ; the solution offers the undoubted advantage of being compatible with existing handling and testing tools.

The heat produced by the IC, and conveyed externally by the heat transfer leads, can be cost effectively transferred to the ambient by means of dedicated copper heatsinks, integrated on the board.

Figure 14 : Medium Power SO and PLCC Frame.



In figure 15, the layout of test boards used for the thermal characterisation of medium power SO-20s (with 8 heat transfer leads) and PLCC-44s (with 11 heat transfer leads) is represented.

The area of the integrated heatsink can be optimised for cost reduction, depending on the dissipation level. In figure 16 the relationship between the Rth(j-a) of the PLCC (33 + 11) and the total dissipating area is given.

It can be noticed that, with 6-7 sq cm of substrate, the thermal resistance of PLCC-44s can be decreased from 55°C/W to 40°C/W, for 1.5-2W dissipation.

A similar performance is possible with the medium power SOs.

Figure 15 : Test Boards for Medium Power SO-20 and PLCC-44 Package.

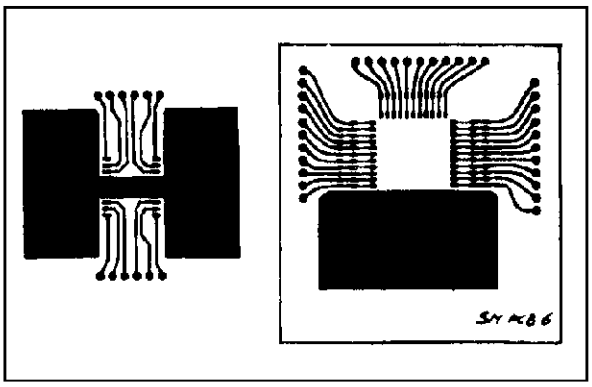
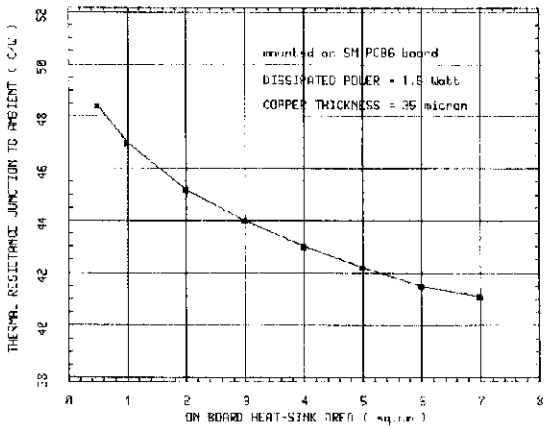


Figure 16 : Rth(j-a) of Medium Power PLCC-44 vs. Dissipating Area on Board.



CONCLUSIONS

In SMT, two main reliability related concerns are resistance to soldering heat and heat dissipation.

RESISTANCE TO SOLDERING HEAT

After extensive evaluation of devices soldered on plastic substrates by means of the three industrial soldering methods (multiple wave soldering, vapour phase and IR reflow), no reliability degradation was found.

The following soldering conditions are possible with SO packaged devices :

- Multiple Wave : T = 250 - 260°C/t = 4s (repetition allowed)
- Vapour Phase : T = 215°C/t = 20s (repetition allowed)
- Infra-red : T > 210°C/t = 60s (Tmax = 225°C)

No crack in the plastic case was evidenced during the above work or in the field, in recent years of production, and no thermal preconditioning was needed. However, this result was obtained after optimisation of the frame design and of the production process. Its extension to the totality of the products existing on the market might be too arbitrary, but it is possible to conclude that the structure of SM packages, when associated with suitable materials and processes, is able to meet the user's requirements.

A similar evaluation is running for PLCC packages and will be completed in the first half of 1988.

HEAT DISSIPATION

Some considerations have been made about the consequence of the lack of some standard evaluation methodology. To standardise test chips and test boards is very important, in order to reach a better knowledge and a better information exchange.

By means of an internally developed test pattern and suitable test boards, three points have been studied :

1. The influence of the substrate on thermal dissipation, whose effect has to be taken into account much more than for insertion packages. With a proper layout it is effective in reducing thermal resistance. For example, dissipation of copper frame SO package can become better than the equivalent Alloy 42 DIP and only 10-20% higher than the equivalent copper DIP.
2. The thermal impedance, whose value is much more suitable for the thermal design of switching applications and can contribute to reduce the cost of the system.
3. The new medium power SO and PLCC packages, which offer the possibility of cost-effective power dissipation in the range of 1.5-2W, still maintaining a standard outline.

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